GIC-00-009B

October 6, 2003

To: Commissioner for Patents
    P.O.Box 1450
    Alexandria, VA 22313-1450

Fr: George O. Saile,   Reg. No. 19,572
    28 Davis Avenue
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Subject:

| Serial No.   10/614,928   07/08/03 |

Jin-Yuan Lee

A STRUCTURE OF HIGH PERFORMANCE
COMBO CHIP AND PROCESSING METHOD

| Grp. Art Unit: |

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation

In An Application.

The following Patents and/or Publications are submitted to

comply with the duty of disclosure under CFR 1.97-1.99 and

37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

1

U.S. Patent 5,811,351 to Kawakita et al., "Semiconductor Device and Method of Manufacturing the Same," discloses a stacked chip structure with bumps on the overlying chip.

U.S. Patent 5,422,435 to Takiar et al., "Stacked Multi-Chip Modules and Method of Manufacturing," discloses a stacked multi-chip module.

U.S. Patent 5,994,166 to Akram et al., "Method of Constructing Stacked Packages," recites a stack chip package using flip chip contacts.

U.S. Patent 5,952,725 to Ball, "Stacked Semiconductor Devices," discloses a stacked chip device with solder ball connectors.

Article, published as part of the 2000 Electronic Components and Technology conference of 05/21/00 through 05/24/00, author: Jean Dufresne, title: "Hybrid Assembly Technology for Flip-Chip-on-Chip (FCOC) Using PBGA Laminate Assembly," Reference number: 0-7803-5908-9/00, IEEE, discloses hybrid assembly technology for flip-chip-on-chip (FCOC) using PBGA laminate assembly.

U.S. Patent 5,608,262 to Degani et al., "Packaging Multi-Chip Modules without Wire-Bond Interconnection," discloses a method and package for packaging multi-chip modules without using wire bond interconnections.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
MEG-00-009B	10/614,928

Applicant: Jin-Yuan Lee

Filing Date	Group Art Unit
07/08/03	

[Stamp: OCT 14 2003 U.S. PATENT & TRADEMARK OFFICE]

U. S. PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5811351	9/22/98	Kawakita et al.	438	613	11/25/97
	5422435	6/6/95	Takiar et al.	174	52.4	5/22/92
	5994166	11/30/99	Akram et al.	438	108	3/10/97
	5952725	9/14/99	Ball	257	777	1/17/97
	5608262	3/4/97	Degani et al.	257	723	2/24/95

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

Article, published as part of the 2000 Electronic Components and Tech. Conf. of 05/21/00 - 05/24/00, by Jean Dufresne, "Hybrid Assembly Technology for Flip-Chip-on-Chip (FCOC) Using PBGA Laminate Assembly," Ref. # 0-7803-5908-9/00, IEEE.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.